TOSHIBA INTEGRATED CIRCUIT

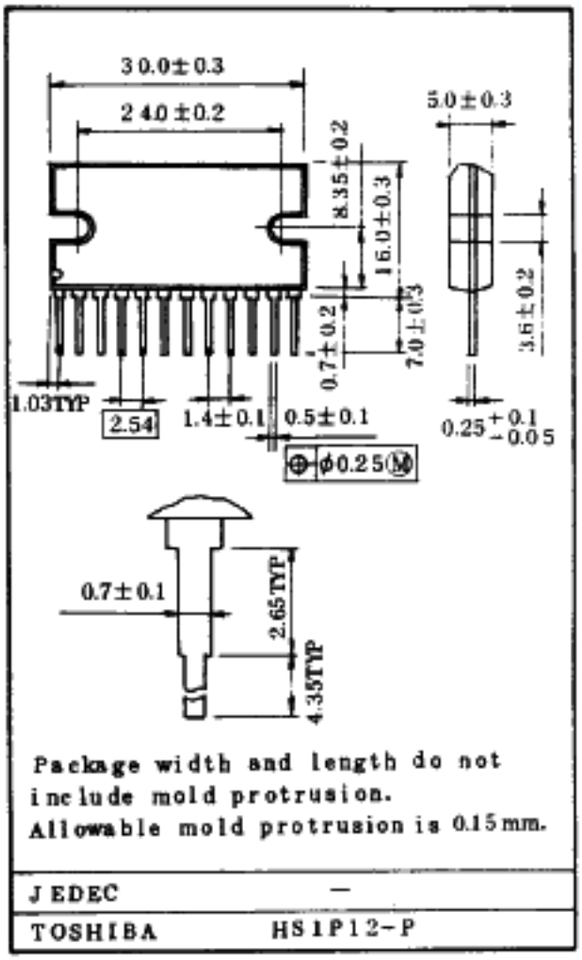
TECHNICAL DATA

TA7240AP, TA7241AP

TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT

SILICON MONOLITHIC

Unit in mm



Package width and length do not include mold protrusion.
Allowable mold protrusion is 0.15mm.

JEDEC	—
TOSHIBA	HS1P12-P

5.8W DUAL AUDIO POWER AMPLIFIER.

19W BTL AUDIO POWER AMPLIFIER.

The TA7240AP/TA7241AP are dual audio power amplifier for consumer applications. It is designed for high power, low distortion and low noise.
It also contains various kind of protectors.
It is suitable for car-audio power amplifier with high performance.

. Two Kinds of Pin Configulation are Available : Normal (TA7240AP) and Reverse (TA7241AP) for Easier Layout Design of Pc-board when Used in BTL-Stereo Application.

. Operating Supply Voltage Range : $V_{CC(opr)}$=9 ~ 18V

. High Power

V_{CC}=13.2V, f=1kHz, R_L=4Ω

BTL	19W (Typ.)	THD=10%
	15W (Typ.)	THD=1%
DUAL	5.8W (Typ.)	THD=10%

· Low Distortion

V_{CC}=13.2V, f=1kHz, R_L=4Ω

BTL	0.03% (TYP.)	P_{OUT}=4W, G_V=40dB
DUAL	0.06% (TYP.)	P_{OUT}=1W, G_V=52dB

· Low Noise

V_{CC}=13.2V, R_L=4Ω

BTL	0.14mV$_{rms}$(TYP.)	G_V=40dB, R_g=0, DIN NOISE : DIN 45405
DUAL	0.7mV$_{rms}$ (TYP.)	G_V=52dB, R_g=10kΩ, BW=20Hz ~ 20kHz

· Protector : Thermal Shut Down, Over Voltage Protection.
BTL-OCL DC Short Protection.

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MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Peak Supply Voltage (0.2 sec)	V_{CC} surge	45	V
DC Supply Voltage	V_{CC} DC	25	V
Operating Supply Voltage	V_{CC} opr	18	V
Output Current (peak)	$I_{O(peak)}$	4.5	A
Power Dissipation	P_D	25	W
Operating Temperature	Topr	-30 ~ 75	°C
Storage Temperature	Tstg	-55 ~ 150	°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_{CC}=13.2V, R_L=4Ω, R_g=600Ω, f=1kHz, Ta=25°C)

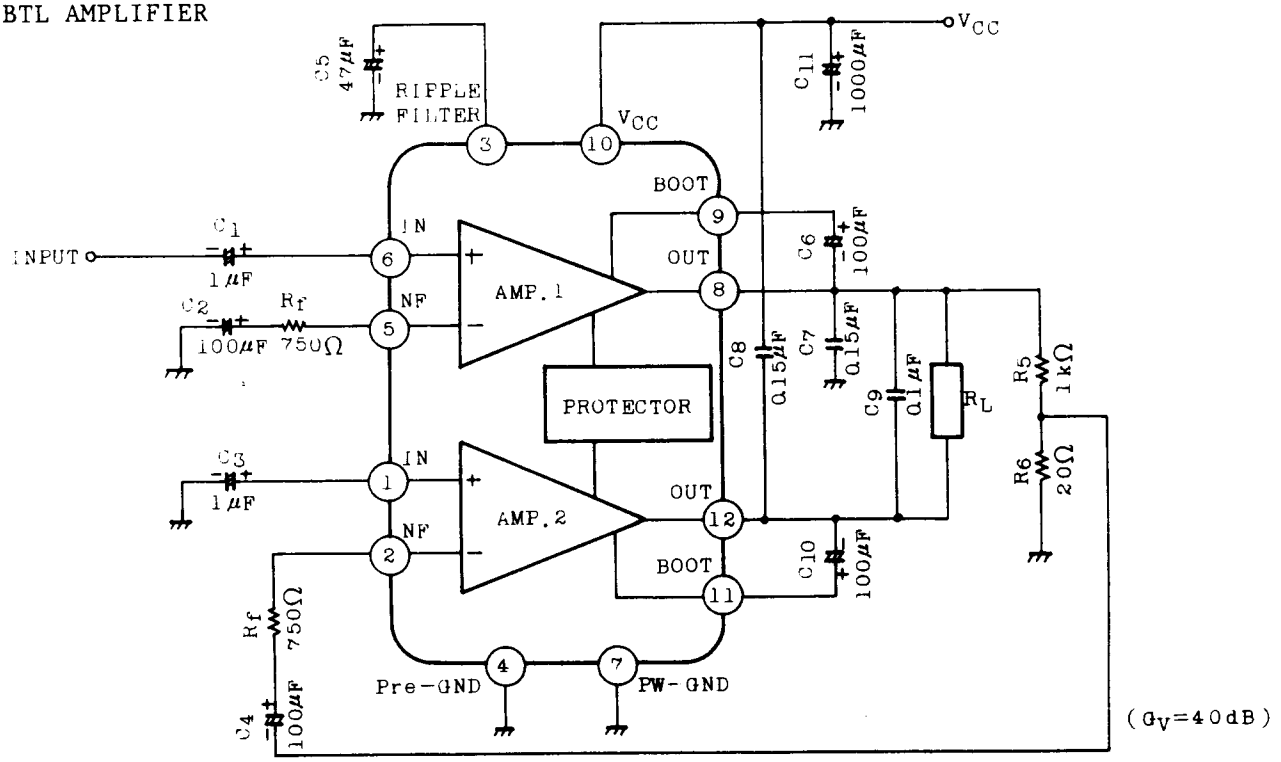
	CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
	Quiescent Current	I_{CCQ}	2	V_{IN}=0	-	80	145	mA
BTL CONNECTION MODE	Output Power	$P_{OUT(1)}$	1	THD=10%	16	19	-	W
		$P_{OUT(2)}$	1	THD=1%	12	15	-	W
	Total Harmonic Distortion	THD(1)	1	P_{OUT}=4W, G_V=40dB	-	0.03	0.25	%
	Output Offset Voltage	V_{OFF}	1	V_{IN}=0	-	0	0.35	V
	Voltage Gain	$G_{V(1)}$	1	V_{OUT}=0dBm	-	40	-	dB
	Output Noise Voltage	$V_{NO(1)}$	1	R_g=0 DIN45405 Noise Filter	-	0.14	-	mVrms
	Ripple Rejection Ratio	R.R(1)	1	f_{ripple}=100Hz V_{ripple}=0dBm	-	-52	-40	dB
DUAL MODE	Output Power	$P_{OUT(3)}$	2	THD=10%	5	5.8	-	W
	Total Harmonic Distortion	THD(2)	2	P_{OUT}=1W	-	0.06	0.30	%
	Voltage Gain	$G_{V(2)}$	2	V_{OUT}=0dBm	50	52	54	dB
	Voltage Gain Ratio	ΔG_V	2	V_{OUT}=0dBm	-1	0	1	dB
	Output Noise Voltage	$V_{NO(2)}$	2	R_g=10kΩ BW=20Hz ~ 20kHz	-	0.7	1.5	mVrms
	Ripple Rejection Ratio	R.R(2)	2	f_{ripple}=100Hz V_{ripple}=0dBm	-	-52	-40	dB
	Cross Talk	C.T	2	V_{OUT}=0dBm	-	-57	-	dB
	Input Resistance	R_{IN}	2	f=1kHz	-	33	-	kΩ

RATION

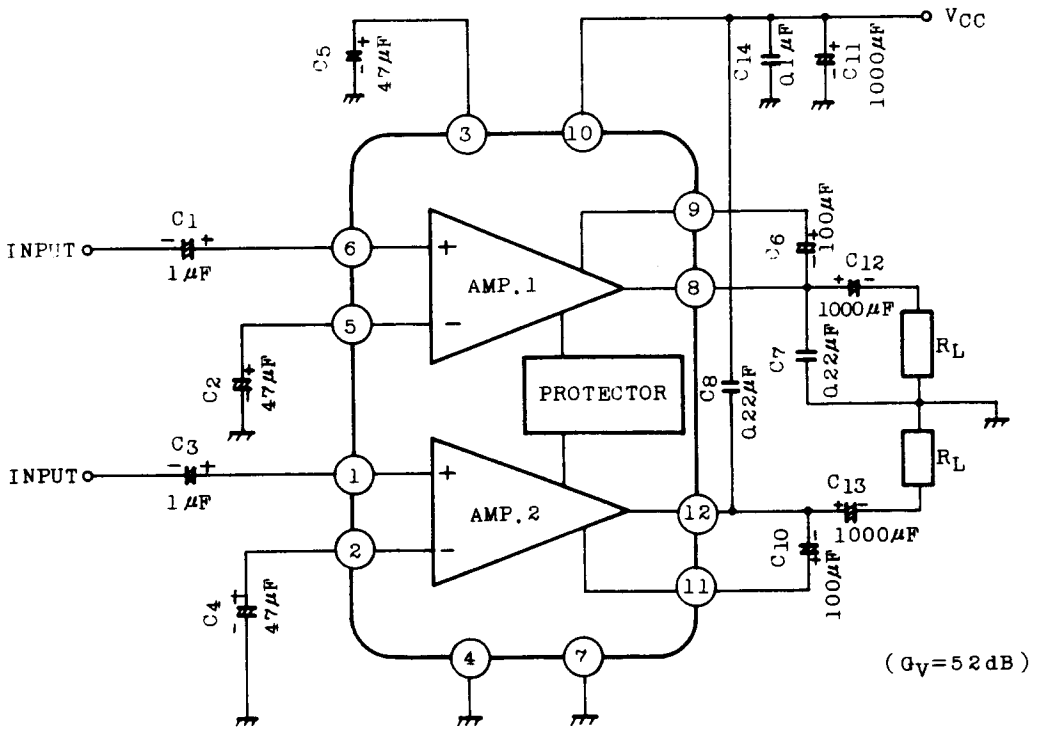
TEST CIRCUIT/APPLICATION CIRCUIT

TA7240AP

(1) BTL AMPLIFIER



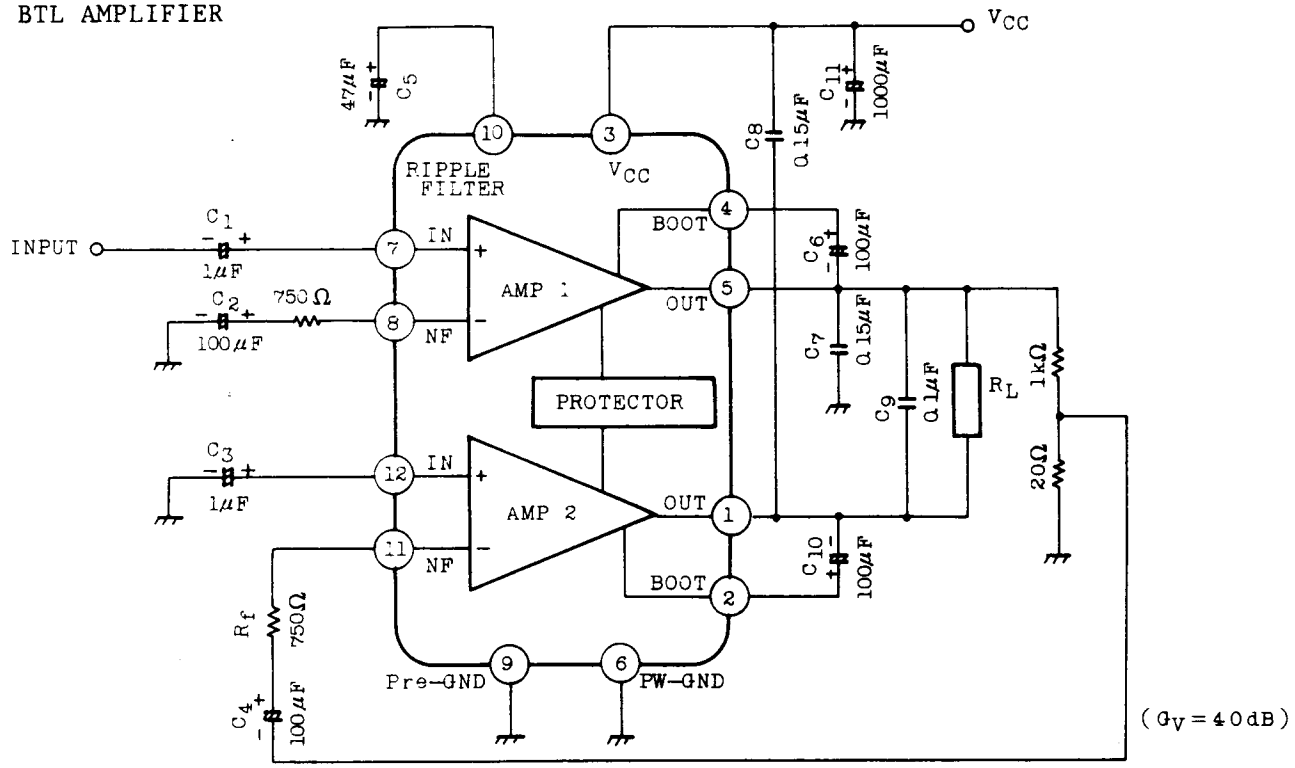
(2) DUAL AMPLIFIER



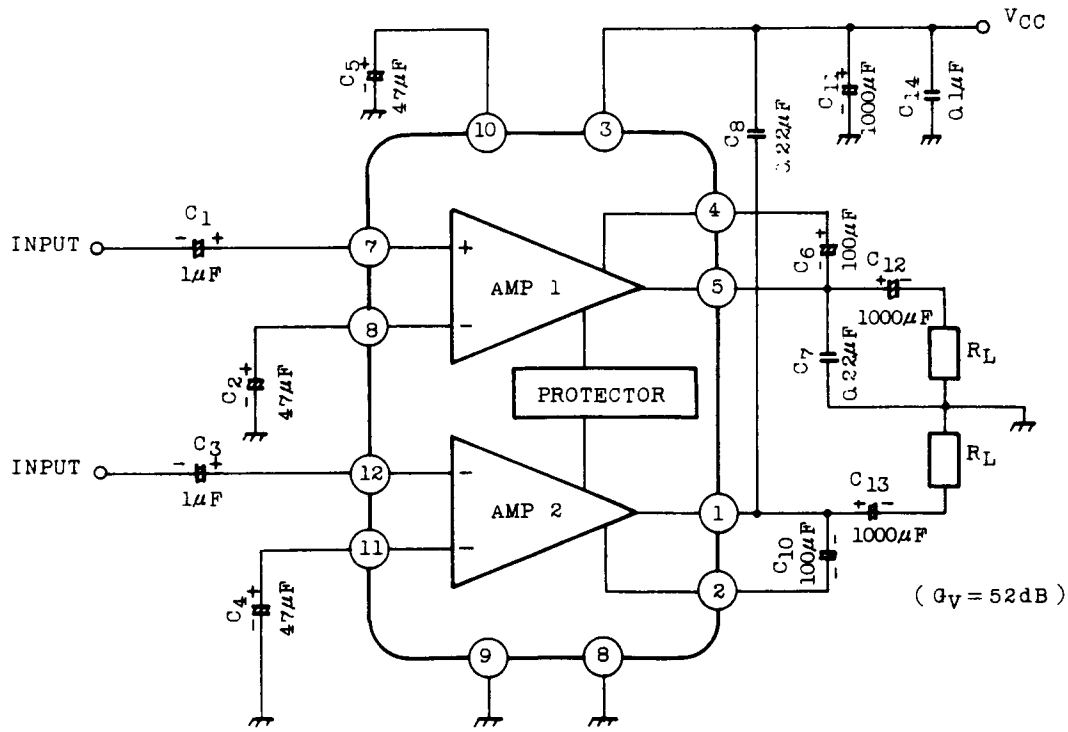
TEST CIRCUIT/APPLICATION CIRCUIT

TA7241AP

(1) BTL AMPLIFIER



(2) DUAL AMPLIFIER



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TYPICAL DC VOLTAGE OF EACH TERMINAL

(V_{CC}=13.2V, Ta=25°C, DUAL MODE TEST CIRCUIT)

TERMINAL No.		1	2	3	4	5	6	7	8	9	10	11	12
DC Voltage (V)	TA7240AP	1.5	1.5	4.4	GND	1.5	1.5	GND	6.6	12.7	V_{CC}	12.7	6.6
	TA7241AP	6.6	12.7	V_{CC}	12.7	6.6	GND	1.5	1.5	GND	4.4	1.5	1.5

APPLICATION INFORMATION

(This explanatory terminal number is for TA7240AP)

1. VOLTAGE GAIN

(1) Dual Mode

The closed loop voltage gain G_V is determined by R_1, R_2, R_3, R_4 and R_f.

$$G_V \fallingdotseq 20\log \frac{R_2+R_f+R_1}{R_f+R_1} + 20\log\frac{R_3+R_4}{R_4} \quad (dB)$$

when R_f=0, G_V=52dB(Typ.)

is given.

The recommended voltage gain is more than 40dB.

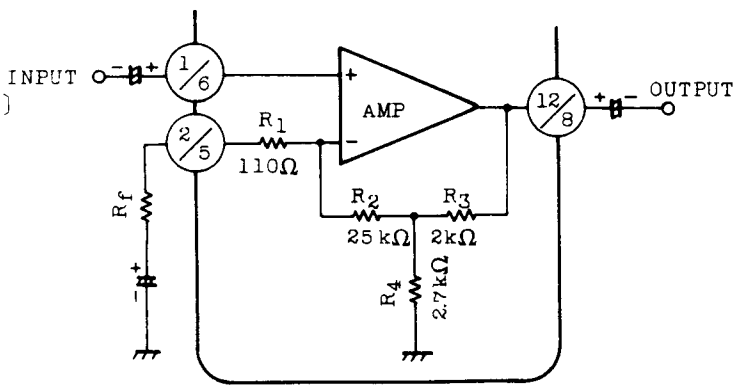


Fig 1

(2) BTL Mode

The recommended BTL connection amplifier is shown in Figure 2.

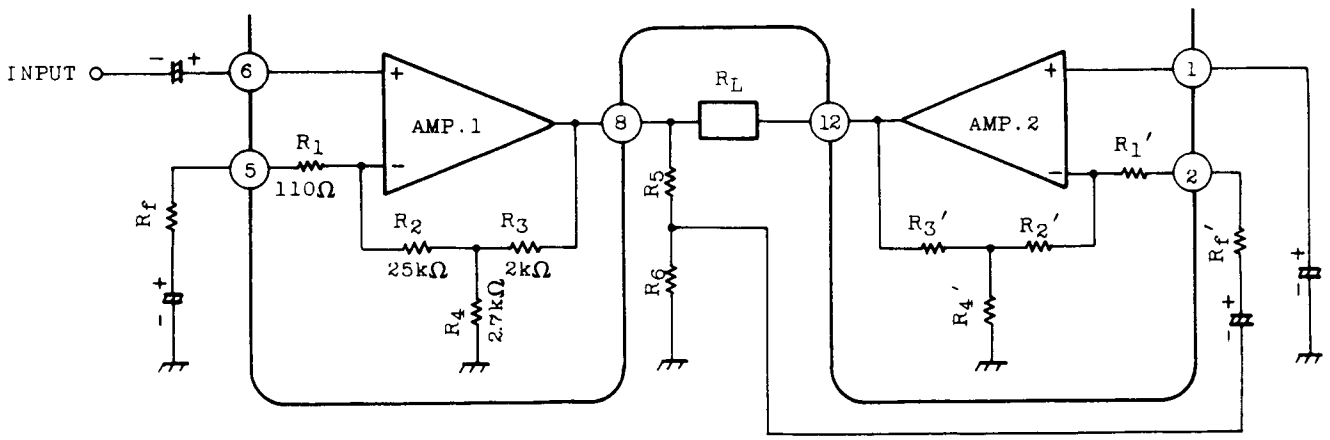


Fig. 2

AMP.1 is noninverting amplifier and AMP.2 is inverting one. The output voltage is divided by resistors R_5 and R_6.

This divided voltage is applied to inverting input of AMP.2. R_5 and R_6 are determined in the following equation.

$$\frac{R_5+R_6}{R_5} = 20 \log \frac{R_1'+R_f'+R_2'}{R_1'+R_f'} + 20 \log \frac{R_3'+R_4'}{R_4'} \quad \text{..... Gv in Dual Mode}$$

The voltage gain in this circuit is 6dB higher than that in dual mode.

$$G_V = 20 \log \frac{R_1+R_f+R_2}{R_1+R_f} + 20 \log \frac{R_3+R_4}{R_4} + 6 \quad [dB]$$

In case of $R_f=0$

$G_V=52+6=58$ [dB]

In case of $R_f=750\Omega$

$G_V=34+6=40$ [dB]

2. MUTING

Audio muting can be accomplished by connecting pin ③ (ripple filter) to GND as shown in Fig.3. Then, the bias circuits are cut off.

Amount of muting attenuation is more than 60dB.

Precaution in muting operation is as follows.

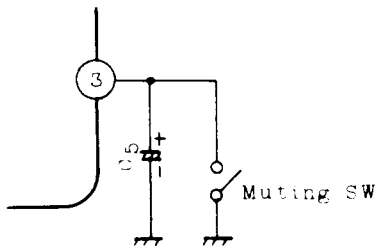


Fig.3

(1) The recovery time at muting off depends on Capacitance C_2, C_4 and C_5 in the test Circuti.

(2) As this muting system is operated by the shart-circuit of ripple filter : C_5, the ripple rejection ratio becomes warse in a muting mode.
Note that some "POP-Noise" occur when bias is shut off with mute-on.

3. CAPACITOR C_7, C_8

The purpose of capacitor C_7, C_8 is to prevent oscillation.

These capacitors need to be small temperature coefficient. So celamic capacitor is unsuitabel.

A voltage gain less than 40dB results occasionally in a parastic oscillation.

Stability for parastic oscillation is promoted by connecting capacitor of 500 ∿ 1000pF between pin ① and pin ② (pin ⑤ and pin ⑥).

The additional capacitors are recommended to be inserted.

4. PRECAUTION AT PRINT BOARD DESIGN

(1) Print Pattern board should be designed in consideration of stability for parastic oscillation.

The following parts-layout is recommended.

1st. Capacitors C_6 and C_{10} are spaced most close to the output pin.

2nd. Capacitor C_7 or C_8 is spaced close to the output pin next to C_6 and C_{10}.

3rd. Capacitor C_9 is spaced close to it next to C_7 and C_8.

4th. Capacitor C_{11} is spaced close to it next to C_9.

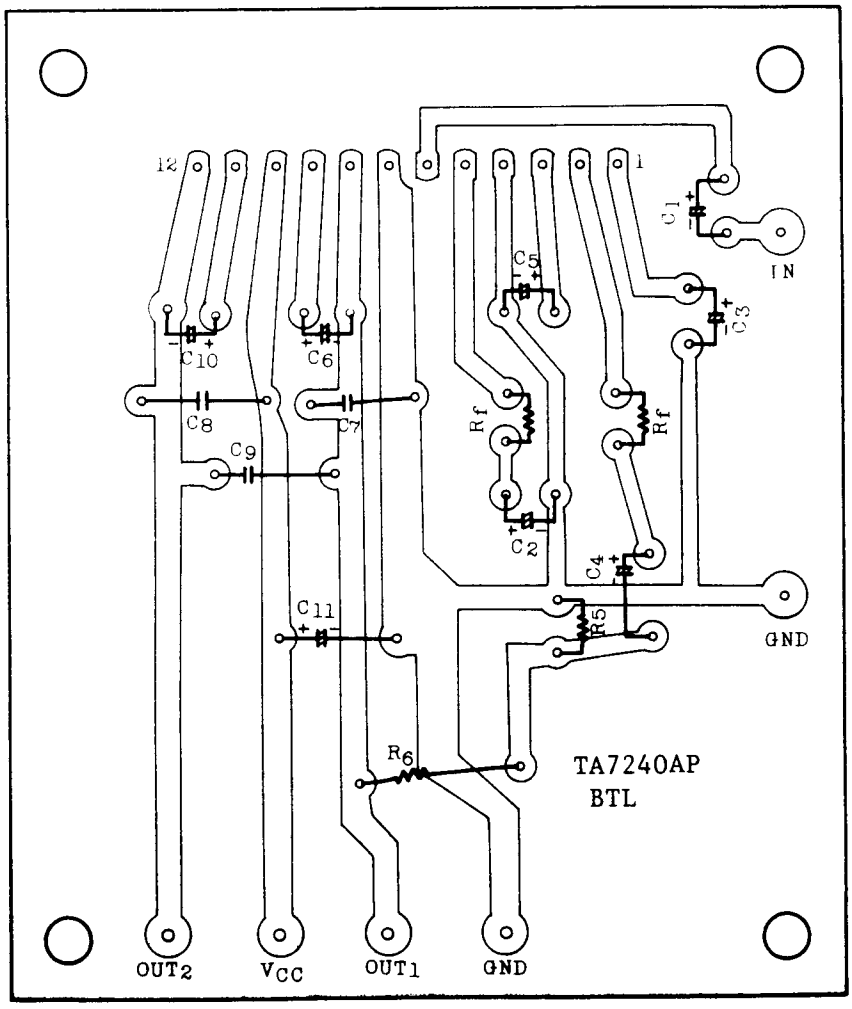
(2) Input line (pin ⑥) and PW-GND line (pin ⑦) should not be spaced in parallel. In the paralled layout, output current signal in PW-GND line is bed back to input line by electromagnetic coupling. Then it deteriorates the total harmonic distortion, especially at high audio frequency region.

(3) Undesirable terminating of capacitors deteriorates "pop" noise or THD. Capacitors C_2, C_4 and C_5 should be terminated to Pre-GND (pin ④). Capacitors C_7, C_{11}, and C_{14} should be terminated to PW-GND (pin ⑦).

(4) It is recommended to refer the standard print board.

STANDARD P.C.B

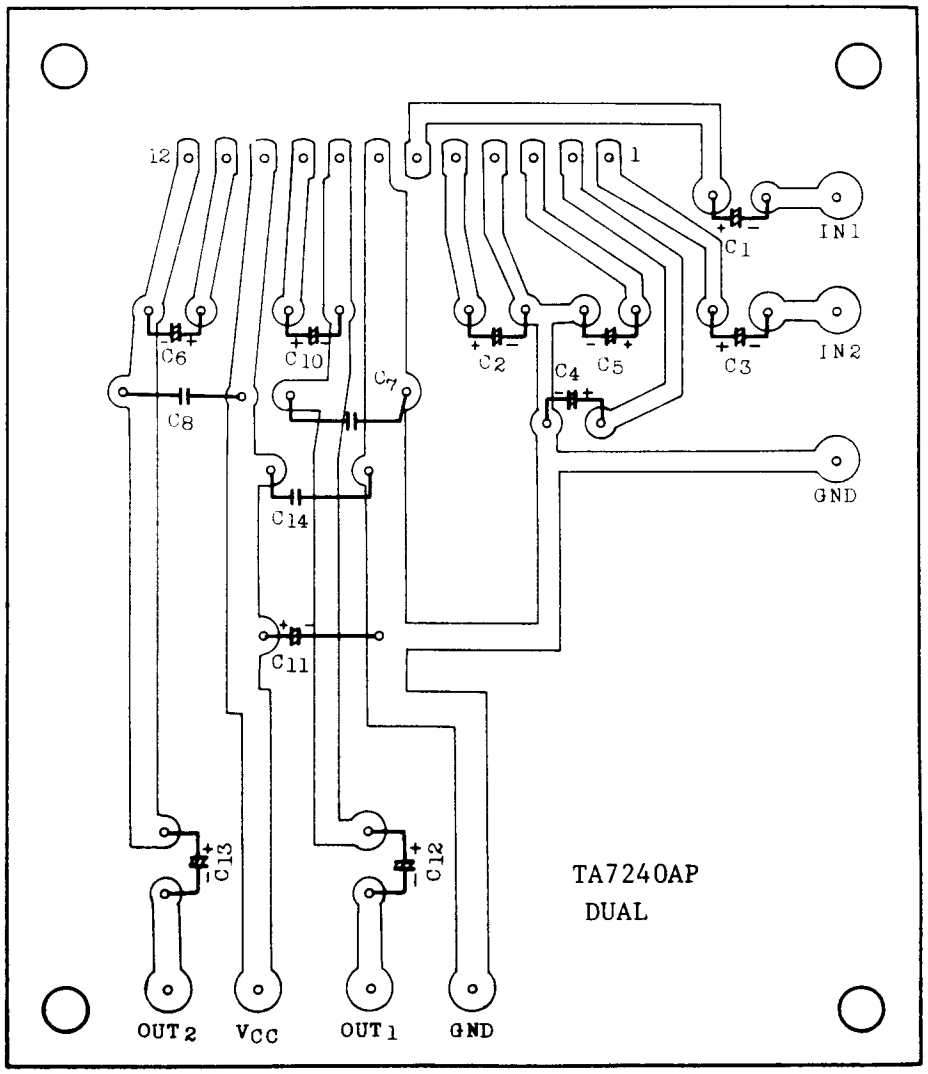
(TA7240AP BTL AMPLIFIER)



BOTTOM VIEW

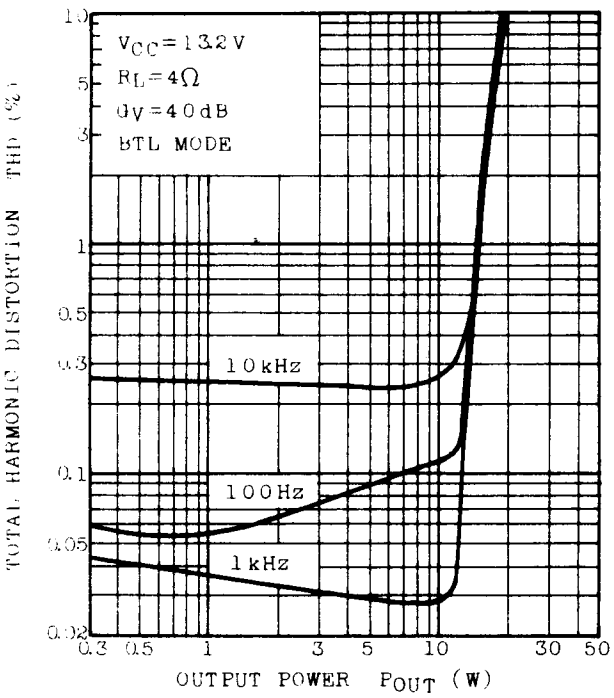
STANDARD P.C.B

(TA7240AP DUAL AMPLIFIER)

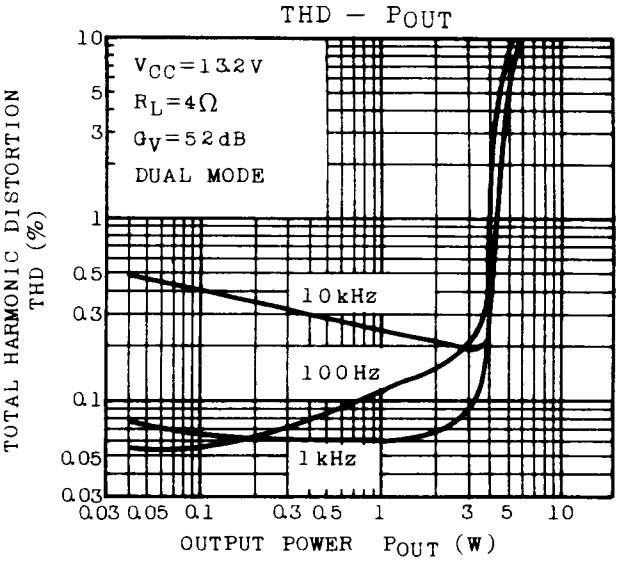


BOTTOM VIEW

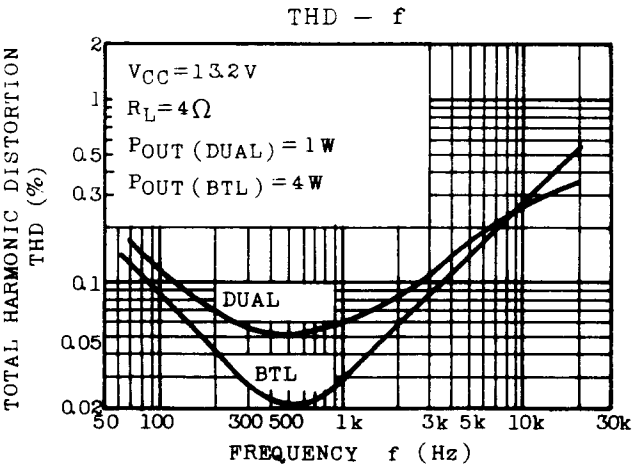
THD – POUT



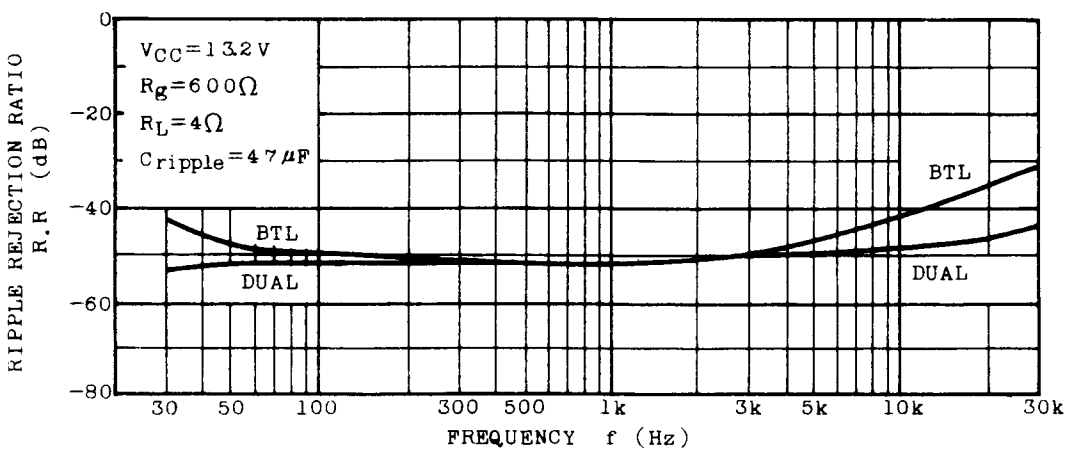
THD – POUT



THD – f



R.R – f



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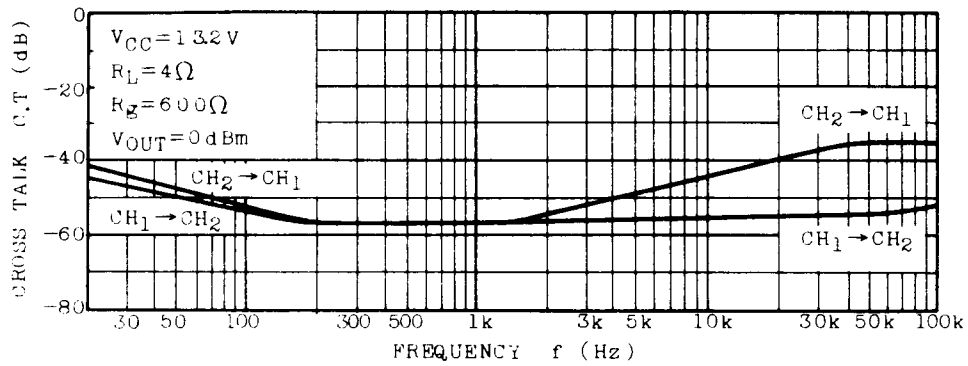
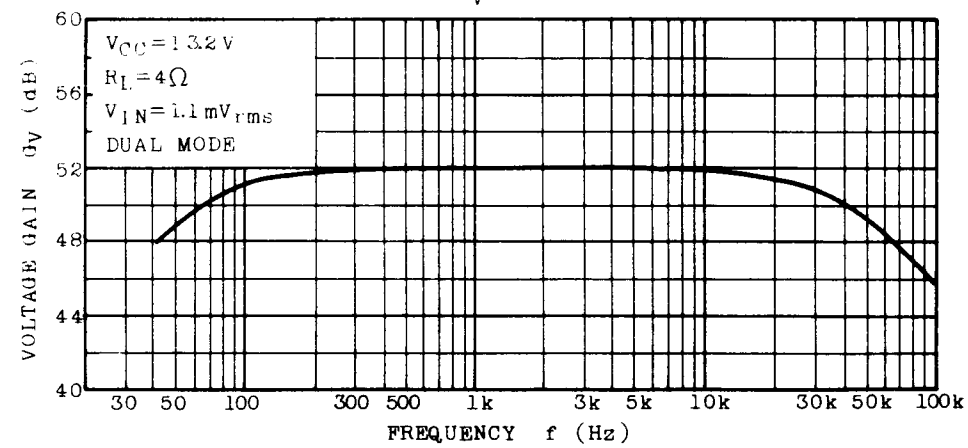
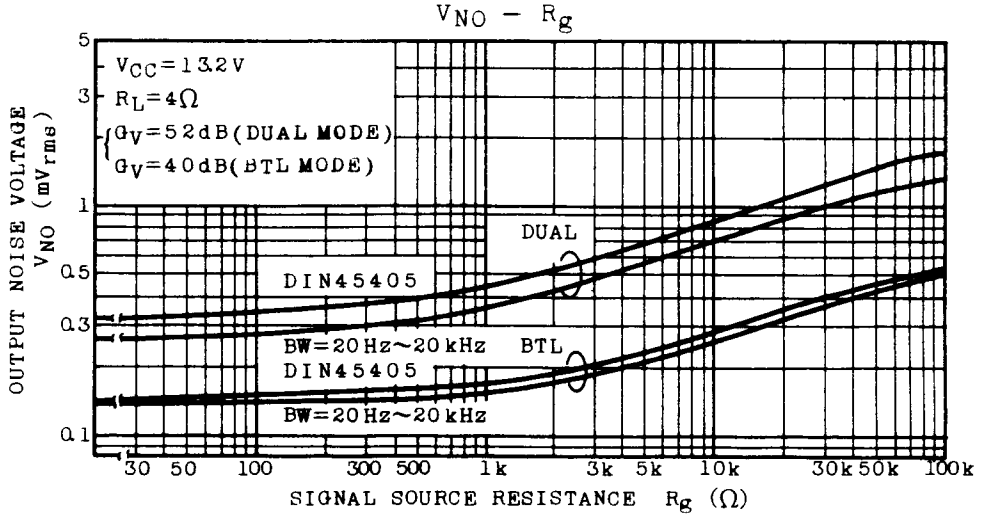
C.T – f



G_V – f



V_{NO} – R_g



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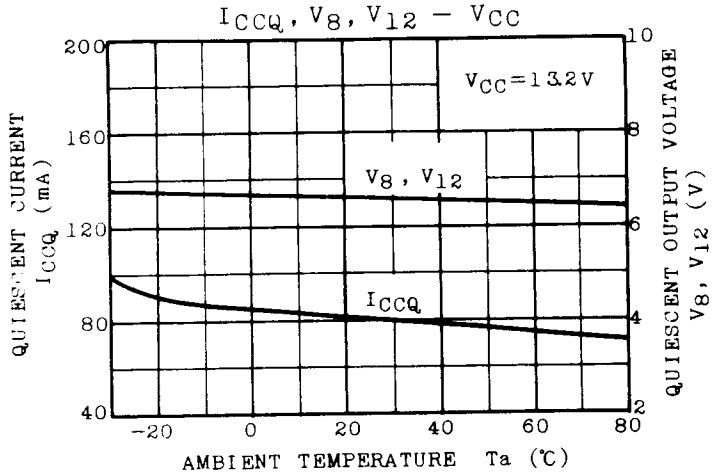
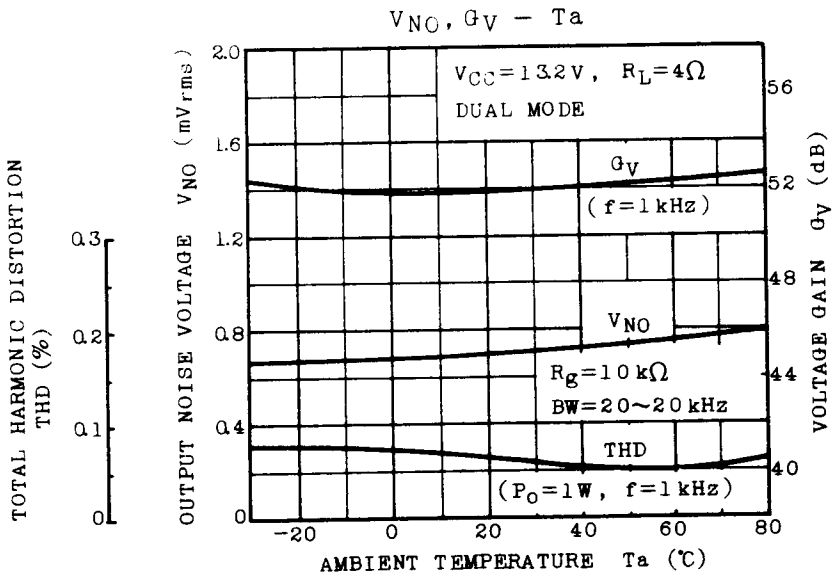
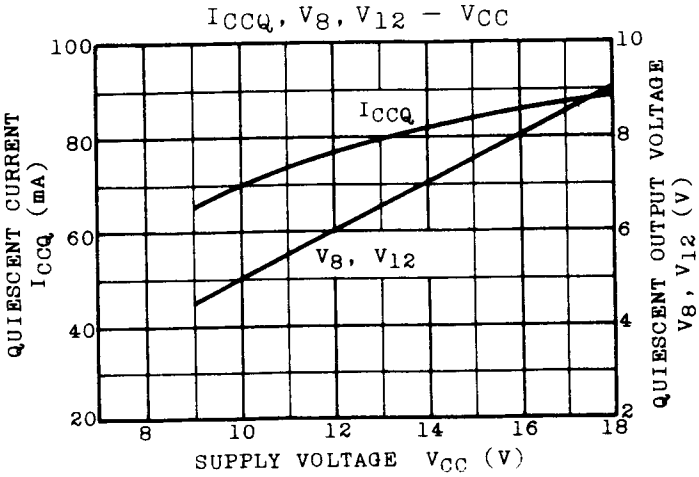
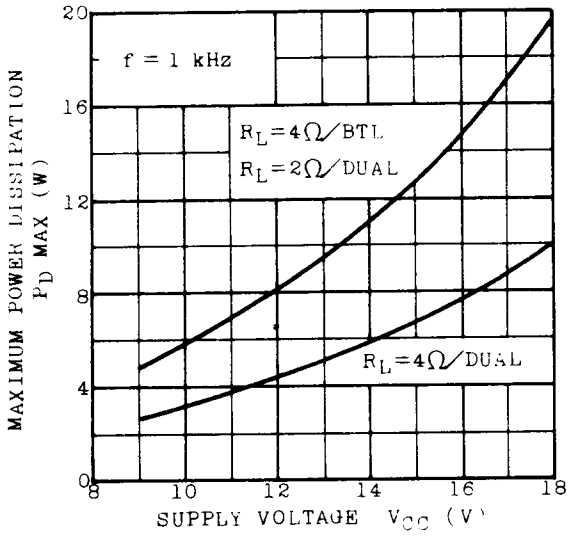

I_{CCQ}, V_8, V_{12} – V_{CC}
V_{CC}=13.2V
V_8, V_{12}
I_{CCQ}
QUIESCENT CURRENT I_{CCQ} (mA)
QUIESCENT OUTPUT VOLTAGE V_8, V_{12} (V)
200
160
120
80
40
10
8
6
4
2
−20
0
20
40
60
80
AMBIENT TEMPERATURE Ta (℃)

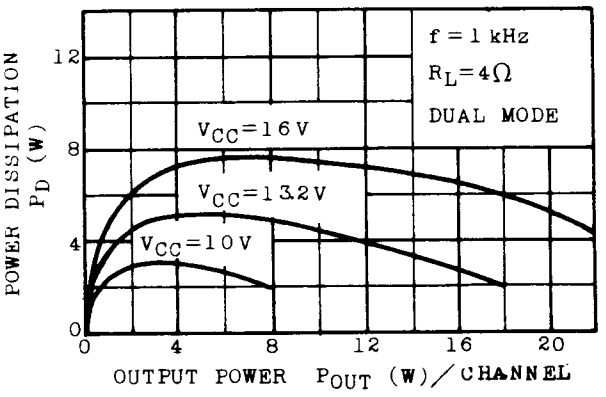

V_{NO}, G_V – Ta
V_{CC}=13.2V, R_L=4Ω
DUAL MODE
G_V
(f=1kHz)
V_{NO}
R_g=10kΩ
BW=20~20kHz
THD
(P_O=1W, f=1kHz)
OUTPUT NOISE VOLTAGE V_{NO} (mVrms)
VOLTAGE GAIN G_V (dB)
TOTAL HARMONIC DISTORTION THD (%)
2.0
1.6
1.2
0.8
0.4
0
56
52
48
44
40
0.3
0.2
0.1
0
−20
0
20
40
60
80
AMBIENT TEMPERATURE Ta (℃)


I_{CCQ}, V_8, V_{12} – V_{CC}
I_{CCQ}
V_8, V_{12}
QUIESCENT CURRENT I_{CCQ} (mA)
QUIESCENT OUTPUT VOLTAGE V_8, V_{12} (V)
100
80
60
40
20
10
8
6
4
2
8
10
12
14
16
18
SUPPLY VOLTAGE V_{CC} (V)

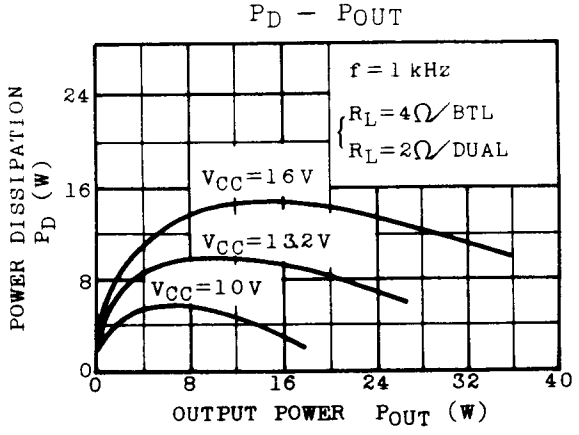
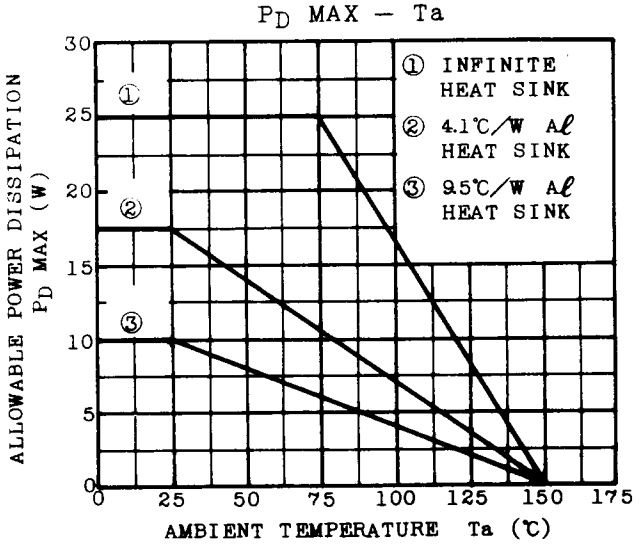
P_D MAX – V_{CC}



P_D – P_{OUT}



P_D – P_{OUT}



P_D MAX – Ta